REMARKS/ARGUMENTS

Applicant received the Office Action dated December 14, 2006 in which the Examiner: 1) rejected claims 1–10 and 9 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent Application Publication No. US 2004/0174831 ("*Yi*") in view of U.S. Patent No. 6,314,504 ("*Dent*"); 2) rejected claims 11, 12, 20, 21 under 35 U.S.C. § 103(a) as being unpatentable over *Yi* in view of *Dent* and U.S. Patent Application Publication No. 2004/0002366 ("*Cromer*"); and 3) rejected claims 13-18 under 35 U.S.C. § 102(e) as being anticipated by *Cromer*.

With this Response, Applicant has amended claims 1-2, 5, 8 and 19. Also, Applicant has cancelled claim 9. Based on the amendments and arguments contained herein, Applicant respectfully requests reconsideration and allowance of the pending claims.

§ 102 REJECTIONS

The Examiner rejected claims 13-18 as being anticipated by *Cromer*. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631. "The identical invention must be shown in as complete detail as is contained in the...claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236.

Cromer fails to teach "configuring the device to interpret read/write commands having a reduced length if the power consumptions parameter exists" as required in claim 13. Instead, *Cromer* teaches that power consumption can be reduced by transmitting data at a lower symbol rate and increasing the number of bits per symbol (see paragraph [0013]). Changing the symbol rate and the number of bits per symbol as in *Cromer* is not related to read/write commands having a reduced length as in claim 13. More specifically, changing the symbol rate simply affects the amount of interference between adjacent symbols and changing the number of bits per symbols is a way of parallelizing bit transmission. Thus, Cromer conserves power by selectively parallelizing

(increasing) bits per symbol instead of reducing the overall number of bits that are interpreted. For at least these reasons, claim 13 and its dependent claims are allowable over *Cromer*.

§ 103 REJECTIONS

The Examiner rejected claims 1-10 and 19 as being unpatentable over *Yi* in view of *Dent*. "To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion of motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art must teach or suggest "all the claim limitations" (MPEP 2143). "The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in the applicant's disclosure." *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

With respect to claim 1, the cited references fail to teach or suggest all the claimed limitations. The Examiner recognizes that *Yi* fails to teach Applicant's "direct memory addressing mode" and "indirect memory addressing mode", and cites *Dent* as teaching these modes. Amended claim 1 requires that "fewer bits are serially transferred between the master device and the slave device for reads and writes in the indirect memory addressing mode than for reads and writes in the direct memory addressing mode." *Dent* does not teach this limitation. Instead, *Dent* shows that 32 bits are used for each of the different addressing modes (see Figure 6). Thus *Dent* does not teach fewer bits are serially transferred during an indirect memory addressing mode. *Yi* is likewise deficient in this regard. For at least this reason, claim 1 and its dependent claims are allowable over *Yi* and *Dent*.

Claim 8 was amended to incorporate the limitations of cancelled claimed 9. Amended claim 8, in part, requires that "the processor and the slave device are configurable to communicate in multiple modes, each mode being associated with a

different read/write command length" where "each read/write command comprises a read/write field, a data length field, and an address field."

The Examiner cites *Dent* as teaching a read/write bit and an address bit and cites *Yi* as teaching a data length field. *Yi* and *Dent*, considered individually or together, still fail to teach or suggest different read/write command lengths where "each read/write command comprises a read/write field, a data length field, and an address field." In *Dent*, 32 bits are used for each of the different addressing modes and thus the overall length of *Dent's* different commands has not changed. Combining *Dent* with *Yi* would not overcome this deficiency. For at least these reasons, claim 8 and its dependent claims are allowable over *Yi* and *Dent*.

Claim 19, in part, requires "means for conveying a "not busy" signal from the slave device to the master device during the first and second modes, the "not busy" signal having fewer bits in the second mode than in the first mode." *Yi* and *Dent*, considered individually or together, fail to teach or suggest this limitation. For at least this reason, claim 19 and its dependent claims are allowable over *Yi* and *Dent*.

CONCLUSION

Applicant respectfully requests reconsideration and that a timely Notice of Allowance be issued in this case. Applicant hereby petitions for any time extensions that are necessary to prevent this case from being abandoned. In the event that additional fees related to this Amendment, or other transactions in this case, are required (including fees for net addition of claims and for time extension), the Examiner is authorized to charge Texas Instruments Incorporated's Deposit Account No. 20-0668 for such fees.

Respectfully submitted,

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